**HM5117805 Series**

16 M EDO DRAM (2-Mword  8-bit) 2 k Refresh

E0156H10 (Ver. 1.0) (Previous ADE-203-630D (Z))

Jun. 27, 2001

### Description

##### The HM5117805 is a CMOS dynamic RAM organized 2,097,152-word  8-bit. It employs the most advanced CMOS technology for high performance and low power. The HM5117805 offers Extended Data Out (EDO) Page Mode as a high speed access mode. Multiplexed address input permits the HM5117805 to be packaged in standard 28-pin plastic SOJ and 28-pin TSOP.

**Features**

* Single 5 V (±10%)
* Access time: 50 ns/60 ns/70 ns (max)
* Power dissipation
  + Active mode: 605 mW/550 mW/495 mW (max)
  + Standby mode : 11 mW (max)

: 0.83 mW (max) (L-version)

* EDO page mode capability
* Long refresh period
  + 2048 refresh cycles : 32 ms

: 128 ms (L-version)

* 4 variations of refresh
  + RAS-only refresh
  + CAS-before-RAS refresh
  + Hidden refresh
  + Self refresh (L-version)
* Battery backup operation (L-version)

Elpida Memory, Inc. is a joint venture DRAM company of NEC Corporation and Hitachi, Ltd.

# HM5117805 Series

|  |  |  |
| --- | --- | --- |
| **Ordering Information**  **Type No.** | **Access time** | **Package** |
| HM5117805J-5 | 50 ns | 400-mil 28-pin plastic SOJ (CP-28DA) |
| HM5117805J-6 | 60 ns |  |
| HM5117805J-7 | 70 ns |  |
| HM5117805LJ-5 | 50 ns |  |
| HM5117805LJ -6 | 60 ns |  |
| HM5117805LJ -7 | 70 ns |  |
| HM5117805S-5 | 50 ns | 300-mil 28-pin plastic SOJ (CP-28DNA) |
| HM5117805S-6 | 60 ns |  |
| HM5117805S-7 | 70 ns |  |
| HM5117805LS-5 | 50 ns |  |
| HM5117805LS-6 | 60 ns |  |
| HM5117805LS-7 | 70 ns |  |
| HM5117805TT-5 | 50 ns | 400-mil 28-pin plastic TSOP II (TTP-28DA) |
| HM5117805TT-6 | 60 ns |  |
| HM5117805TT-7 | 70 ns |  |
| HM5117805LTT-5 | 50 ns |  |
| HM5117805LTT-6 | 60 ns |  |
| HM5117805LTT-7 | 70 ns |  |
| HM5117805TS-5 | 50 ns | 300-mil 28-pin plastic TSOP II (TTP-28DB) |
| HM5117805TS-6 | 60 ns |  |
| HM5117805TS-7 | 70 ns |  |
| HM5117805LTS-5 | 50 ns |  |
| HM5117805LTS-6 | 60 ns |  |
| HM5117805LTS-7 | 70 ns |  |

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# HM5117805 Series

### Pin Arrangement

HM5117805J/LJ Series HM5117805S/LS Series

HM5117805TT/LTT Series HM5117805TS/LTS Series

V

CC

V

SS

VCC

I/O0 I/O1 I/O2 I/O3 WE RAS NC A10 A0 A1 A2

A3

VCC

VSS

V

CC

VSS I/O7

I/O6 I/O5 I/O4 CAS OE A9 A8 A7 A6 A5 A4 VSS

(Top view)

(Top view)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| I/O0 |  | 2 | 27 |  | I/O7 |
| I/O1 |  | 3 | 26 |  | I/O6 |
| I/O2 |  | 4 | 25 |  | I/O5 |
| I/O3 |  | 5 | 24 |  | I/O4 |
| WE |  | 6 | 23 |  | CAS |
| RAS |  | 7 | 22 |  | OE |
| NC |  | 8 | 21 |  | A9 |
| A10 |  | 9 | 20 |  | A8 |
| A0 |  | 10 | 19 |  | A7 |
| A1 |  | 11 | 18 |  | A6 |
| A2 |  | 12 | 17 |  | A5 |
| A3 |  | 13 | 16 |  | A4 |

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | |  |
|  | 1 | 28 |  |
|  | 2 | 27 |  |
|  | 3 | 26 |  |
|  | 4 | 25 |  |
|  | 5 | 24 |  |
|  | 6 | 23 |  |
|  | 7 | 22 |  |
|  | 8 | 21 |  |
|  | 9 | 20 |  |
|  | 10 | 19 |  |
|  | 11 | 18 |  |
|  | 12 | 17 |  |
|  | 13 | 16 |  |
|  | 14 | 15 |  |
|  |  | |  |

**Pin Description**

1

28

14

15



###### Pin name Function

A0 to A10 Address input

* Row/Refresh address A0 to A10
* Column address I/O0 to I/O7 Data input/Data output RAS Row address strobe

CAS Column address strobe

WE Read/Write enable

OE Output enable

VCC Power supply

VSS Ground

NC No connection

A0 to A9

Data Sheet E0156H10

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# HM5117805 Series

Column address buffers

•

•

•

Row address buffers

•

•

•

### Block Diagram

RAS

CAS

WE

OE

A0 A1

to

A9

I/O0

to I/O7

A10

I/O buffers

Timing and control

|  |  |
| --- | --- |
|  | Column decoder |
| Row decoder | 2M array |
| 2M array |
| 2M array |
| 2M array |
| 2M array |
| 2M array |
| 2M array |
| 2M array |

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# HM5117805 Series

|  |  |  |  |
| --- | --- | --- | --- |
| **Absolute Maximum Ratings**  **Parameter** | **Symbol** | **Value** | **Unit** |
| Voltage on any pin relative to VSS | VT | –1.0 to +7.0 | V |
| Supply voltage relative to VSS | VCC | –1.0 to +7.0 | V |
| Short circuit output current | Iout | 50 | mA |
| Power dissipation | PT | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | –55 to +125 | °C |

**Recommended DC Operating Conditions** (Ta = 0 to +70°C)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter Symbol** | **Min** | **Typ** | **Max** | **Unit** | **Note** |
| Supply voltage VCC | 4.5 | 5.0 | 5.5 | V | 1 |
| Input high voltage VIH | 2.4 | — | 6.5 | V | 1 |
| Input low voltage VIL | –1.0 | — | 0.8 | V | 1 |
| Note: 1. All voltage referred to VSS. |  |  |  |  |  |

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# HM5117805 Series

**DC Characteristics** (Ta = 0 to +70°C, VCC = 5 V ± 10%, VSS = 0 V)

###### HM5117805

CC5 IH

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | | **-5** |  | **-6** |  | **-7** |  | | |
| **Parameter Symbol** | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit Test conditions** | |
| Operating current\*1, \*2 I  CC1 | | — | 110 | — | 100 | — | 90 | mA tRC = min | |
| Standby current ICC2 | | — | 2 | — | 2 | — | 2 | mA TTL interface  RAS, CAS = VIH  Dout = High-Z | |
|  | | — | 1 | — | 1 | — | 1 | mA CMOS interface  RAS, CAS  VCC – 0.2 V  Dout = High-Z | |
| Standby current ICC2  (L-version) | | — | 150 | — | 150 | — | 150 | µA CMOS interface  RAS, CAS  VCC – 0.2 V  Dout = High-Z | |
| RAS-only refresh current\*2 I  CC3 | | — | 110 | — | 100 | — | 90 | mA tRC = min | |
| Standby current\*1 I | | — | 5 | — | 5 | — | 5 | mA RAS = V  CAS = VIL  Dout = enable | |
| CAS-before-RAS refresh ICC6  current | | — | 110 | — | 100 | — | 90 | mA tRC = min | |
| EDO page mode ICC7  current\*1, \*3 | | — | 100 | — | 90 | — | 85 | mA tHPC = min | |
| Battery backup current\*4 I | | — | 500 | — | 500 | — | 500 | µA CMOS interface | |
|  |  |  |  |  |  |  |  |  |  |
| (Standby with CBR refresh) |  |  |  |  |  |  |  |  | Dout = High-Z |
| (L-version) |  |  |  |  |  |  |  |  | CBR refresh: |
|  |  |  |  |  |  |  |  |  | tRC = 62.5 µs tRAS  0.3 µs |
| Self refresh mode current (L-version) | ICC11 | — | 300 | — | 300 | — | 300 | µA | CMOS interface  RAS, CAS  0.2V |
|  |  |  |  |  |  |  |  |  | Dout = High-Z |
| Input leakage current | ILI | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V  Vin  7 V |
| Output leakage current | ILO | –10 | 10 | –10 | 10 | –10 | 10 | µA | 0 V  Vout  7 V Dout = disable |
| Output high voltage | VOH | 2.4 | VCC | 2.4 | VCC | 2.4 | VCC | V | High Iout = –2 mA |
| Output low voltage | VOL | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

CC10

Notes: 1. ICC depends on output load condition when the device is selected. ICC max is specified at the output open condition.

1. Address can be changed once or less while RAS = VIL.
2. Address can be changed once or less while CAS = VIH.
3. CAS = L ( 0.2 V) while RAS = L ( 0.2 V).

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# HM5117805 Series

**Capacitance** (Ta = 25°C, VCC = 5 V ± 10%)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Typ** | **Max** | **Unit** | **Notes** |
| Input capacitance (Address) | CI1 | — | 5 | pF | 1 |
| Input capacitance (Clocks) | CI2 | — | 7 | pF | 1 |
| Output capacitance (Data-in, Data-out) | CI/O | — | 7 | pF | 1, 2 |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS = VIH to disable Dout.

**AC Characteristics** (Ta = 0 to +70°C, VCC = 5 V ±10%, VSS = 0 V)

\*1, \*2, \*18

#### Test Conditions

##### Input rise and fall time: 2 ns

* Input levels: VIL = 0 V, VIH = 3 V
* Input timing reference levels: 0.8 V, 2.4 V
* Output timing reference levels: 0.8 V, 2.0 V
* Output load: 1 TTL gate + CL (100 pF) (Including scope and jig)

Data Sheet E0156H10

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# HM5117805 Series

#### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

###### HM5117805

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | | **-5** |  | **-6** |  | **-7** |  | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Random read or write cycle time | tRC | 84 | — | 104 | — | 124 | — | ns |  |
| RAS precharge time | tRP | 30 | — | 40 | — | 50 | — | ns |  |
| CAS precharge time | tCP | 7 | — | 10 | — | 13 | — | ns |  |
| RAS pulse width | tRAS | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |  |
| CAS pulse width | tCAS | 7 | 10000 | 10 | 10000 | 13 | 10000 | ns |  |
| Row address setup time | tASR | 0 | — | 0 | — | 0 | — | ns |  |
| Row address hold time | tRAH | 7 | — | 10 | — | 10 | — | ns |  |
| Column address setup time | tASC | 0 | — | 0 | — | 0 | — | ns |  |
| Column address hold time | tCAH | 7 | — | 10 | — | 13 | — | ns |  |
| RAS to CAS delay time | tRCD | 11 | 37 | 14 | 45 | 14 | 52 | ns | 3 |
| RAS to column address delay time | tRAD | 9 | 25 | 12 | 30 | 12 | 35 | ns | 4 |
| RAS hold time | tRSH | 10 | — | 13 | — | 13 | — | ns |  |
| CAS hold time | tCSH | 35 | — | 40 | — | 45 | — | ns |  |
| CAS to RAS precharge time | tCRP | 5 | — | 5 | — | 5 | — | ns |  |
| OE to Din delay time | tOED | 13 | — | 15 | — | 18 | — | ns | 5 |
| OE delay time from Din | tDZO | 0 | — | 0 | — | 0 | — | ns | 6 |
| CAS delay time from Din | tDZC | 0 | — | 0 | — | 0 | — | ns | 6 |
| Transition time (rise and fall) | tT | 2 | 50 | 2 | 50 | 2 | 50 | ns | 7 |

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# HM5117805 Series

#### Read Cycle

###### HM5117805

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **-5** |  | **-6** |  | **-7** |  |  |  |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Access time from RAS | tRAC | — | 50 | — | 60 | — | 70 | ns | 8, 9 |
| Access time from CAS | tCAC | — | 13 | — | 15 | — | 18 | ns | 9, 10, 17 |
| Access time from address | tAA | — | 25 | — | 30 | — | 35 | ns | 9, 11, 17 |
| Access time from OE | tOEA | — | 13 | — | 15 | — | 18 | ns | 9 |
| Read command setup time | tRCS | 0 | — | 0 | — | 0 | — | ns |  |
| Read command hold time to CAS | tRCH | 0 | — | 0 | — | 0 | — | ns | 12 |
| Read command hold time from RAS | tRCHR | 50 | — | 60 | — | 70 | — | ns |  |
| Read command hold time to RAS | tRRH | 0 | — | 0 | — | 0 | — | ns | 12 |
| Column address to RAS lead time | tRAL | 25 | — | 30 | — | 35 | — | ns |  |
| Column address to CAS lead time | tCAL | 15 | — | 18 | — | 23 | — | ns |  |
| CAS to output in low-Z | tCLZ | 0 | — | 0 | — | 0 | — | ns |  |
| Output data hold time | tOH | 3 | — | 3 | — | 3 | — | ns | 20 |
| Output data hold time from OE | tOHO | 3 | — | 3 | — | 3 | — | ns |  |
| Output buffer turn-off time | tOFF | — | 13 | — | 15 | — | 15 | ns | 13, 20 |
| Output buffer turn-off to OE | tOEZ | — | 13 | — | 15 | — | 15 | ns | 13 |
| CAS to Din delay time | tCDD | 13 | — | 15 | — | 18 | — | ns | 5 |
| Output data hold time from RAS | tOHR | 3 | — | 3 | — | 3 | — | ns | 20 |
| Output buffer turn-off to RAS | tOFR | — | 13 | — | 15 | — | 15 | ns | 20 |
| Output buffer turn-off to WE | tWEZ | — | 13 | — | 15 | — | 15 | ns |  |
| WE to Din delay time | tWED | 13 | — | 15 | — | 18 | — | ns |  |
| RAS to Din delay time | tRDD | 13 | — | 15 | — | 18 | — | ns |  |
| RAS next CAS delay time | tRNCD | 50 | — | 60 | — | 70 | — | ns |  |

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#### Write Cycle

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **HM5117805** | | | | | | | | | |
|  |  | **-5** |  | **-6** |  | **-7** |  |  |  |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Write command setup time | tWCS | 0 | — | 0 | — | 0 | — | ns | 14 |
| Write command hold time | tWCH | 7 | — | 10 | — | 13 | — | ns |  |
| Write command pulse width | tWP | 7 | — | 10 | — | 10 | — | ns |  |
| Write command to RAS lead time | tRWL | 7 | — | 10 | — | 13 | — | ns |  |
| Write command to CAS lead time | tCWL | 7 | — | 10 | — | 13 | — | ns |  |
| Data-in setup time | tDS | 0 | — | 0 | — | 0 | — | ns | 15 |
| Data-in hold time | tDH | 7 | — | 10 | — | 13 | — | ns | 15 |
| **Read-Modify-Write Cycle** |  |  |  |  |  |  |  |  |  |
| **HM5117805** | | | | | | | | | |
|  |  | **-5** |  | **-6** |  | **-7** |  |  |  |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Read-modify-write cycle time | tRWC | 111 | — | 135 | — | 161 | — | ns |  |
| RAS to WE delay time | tRWD | 67 | — | 79 | — | 92 | — | ns | 14 |
| CAS to WE delay time | tCWD | 30 | — | 34 | — | 40 | — | ns | 14 |
| Column address to WE delay time | tAWD | 42 | — | 49 | — | 57 | — | ns | 14 |
| OE hold time from WE | tOEH | 13 | — | 15 | — | 18 | — | ns |  |
| **Refresh Cycle** |  |  |  |  |  |  |  |  |  |
| **HM5117805** | | | | | | | | | |
|  | | **-5** |  | **-6** |  | **-7** |  |  |  |
| **Parameter Symbol** | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| CAS setup time (CBR refresh cycle) tCSR | | 5 | — | 5 | — | 5 | — | ns |  |
| CAS hold time (CBR refresh cycle) tCHR | | 7 | — | 10 | — | 10 | — | ns |  |
| WE setup time (CBR refresh cycle) tWRP | | 0 | — | 0 | — | 0 | — | ns |  |
| WE hold time (CBR refresh cycle) tWRH | | 7 | — | 10 | — | 10 | — | ns |  |
| RAS precharge to CAS hold time tRPC | | 5 | — | 5 | — | 5 | — | ns |  |

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#### EDO Page Mode Cycle

###### HM5117805

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **-5** |  | **-6** |  | **-7** |  |  |  |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| EDO page mode cycle time | tHPC | 20 | — | 25 | — | 30 | — | ns | 19 |
| EDO page mode RAS pulse width | tRASP | — | 100000 | — | 100000 | — | 100000 | ns | 16 |
| Access time from CAS precharge | tCPA | — | 28 | — | 35 | — | 40 | ns | 9, 17 |
| RAS hold time from CAS precharge | tCPRH | 28 | — | 35 | — | 40 | — | ns |  |
| Output data hold time from CAS low | tDOH | 3 | — | 3 | — | 3 | — | ns | 9, 17 |
| CAS hold time referred OE | tCOL | 7 | — | 10 | — | 13 | — | ns |  |
| CAS to OE setup time | tCOP | 5 | — | 5 | — | 5 | — | ns |  |
| Read command hold time from CAS  precharge | tRCHC | 28 | — | 35 | — | 40 | — | ns |  |

**EDO Page Mode Read-Modify-Write Cycle**

**HM5117805**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | | **-5** |  | **-6** |  | **-7** |  | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| EDO page mode read- modify-write cycle time | tHPRWC | 57 | — | 68 | — | 79 |  | ns |  |
| WE delay time from CAS precharge | tCPW | 45 | — | 54 | — | 62 |  | ns | 14 |
| **Refresh** |  |  |  |  |  |  |  |  |  |
| **Parameter** | **Symbol** | | **Max** | | **Unit** | | **Note** | | |
| Refresh period | tREF | | 32 | | ms | | 2048 cycles | | |
| Refresh period (L-version) | tREF | | 128 | | ms | | 2048 cycles | | |

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Self Refresh Mode (L-version)** |  |  |  | | | | |
|  |  | **HM5117805L** |
|  |  | **-5** | **-6** |  | **-7** |  |  |
| **Parameter** | **Symbol** | **Min Max** | **Min** | **Max** | **Min** | **Max** | **Unit Notes** |
| RAS pulse width (self refresh) | tRASS | 100 — | 100 | — | 100 | — | µs |
| RAS precharge time (self refresh) | tRPS | 90 — | 110 | — | 130 | — | ns |
| CAS hold time (self refresh) | tCHS | –50 — | –50 | — | –50 | — | ns |

Notes: 1. AC measurements assume tT = 2 ns.

1. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles are required.
2. Operation with the tRCD (max) limit insures that tRAC (max) can be met, tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
3. Operation with the tRAD (max) limit insures that tRAC (max) can be met, tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, then access time is controlled exclusively by tAA.
4. Either tOED or tCDD must be satisfied.
5. Either tDZO or tDZC must be satisfied.
6. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH (min) and VIL (max).
7. Assumes that tRCD  tRCD (max) and tRAD  tRAD (max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.
8. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
9. Assumes that tRCD  tRCD (max) and tRAD  tRAD (max).
10. Assumes that tRCD  tRCD (max) and tRAD  tRAD (max).
11. Either tRCH or tRRH must be satisfied for a read cycles.
12. tOFF (max) and tOEZ (max) define the time at which the outputs achieve the open circuitconditionand are not referred to output voltage levels.
13. tWCS, tRWD, tCWD, tAWD and tCPW are not restrictive operating parameters. They are included inthe data sheet as electrical characteristics only; if tWCS  tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tRWDtRWD(min), tCWD  tCWD (min), and tAWD  tAWD (min), ortCWD  tCWD (min), tAWD  tAWD (min) and tCPW  tCPW (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. These parameters are referred to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
15. tRASP defines RAS pulse width in EDO page mode cycles.
16. Access time is determined by the longest among tAA, tCAC and tCPA.
17. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
18. tHPC (min) can be achieved during a series of EDO page mode write cycles or EDO pagemode read cycles. If both write and read operation are mixed in a EDO page mode RAS cycle (EDO page mode mix cycle (1), (2)), minimum value of CAS cycle (tCAS + tCP + 2 tT) becomes greater than the specified tHPC (min) value.The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).

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1. Data output turns off and becomes high impedance fromlater rising edge of RAS and CAS . Hold time and turn off time are specified by the timing specifications of later rising edge of RAS and CAS between tOHR and tOH and between tOFR and tOFF.
2. Please do not use tRASS timing, 10 µs  tRASS  100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If tRASS  100 µs, then RAS precharge time should use tRPS instead of tRP.
3. If you use RAS only refresh or CBR burst refresh mode in normal read/write cycles, 2048 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
4. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
5. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit fromself fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
6. XXX: H or L (H: VIH (min)  VIN  VIH (max), L: VIL (min)  VIN  VIL (max))

///////: Invalid Dout

When the address, clock and input pins are not described on timing waveforms, their pins must be applied VIH or VIL.

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### Timing Waveforms\*25

#### Read Cycle

t RC

t RAS

t RP

t CSH

t CRP

t RCD

t T

t RSH

t CAS

t RAD

t ASR

t

t RAL

t CAL

t ASC t CAH

RAH

Row

Column

t RRH

t RCHR

t RCS

t RCH

t WED

t DZC

t CDD

t RDD

High-Z

t DZO t OEA

t OED

t CAC

t AA

t RAC

t CLZ

t OEZ

t OHO

t OFF

t OH

t OFR

t OHR

t WEZ

Dout

RAS

CAS

Address

WE

Din

OE

Dout

Data Sheet E0156H10

14

#### Early Write Cycle

tRC

tRAS

tRP

tCSH

tCRP

tRCD

tT

tRSH

tCAS

tASR tRAH

tASC tCAH

Row

Column

tWCS

tWCH

tDS

tDH

Din

RAS

CAS

Address

WE

Din

Dout

High-Z\*

\* t WCS tWCS (min)

Data Sheet E0156H10

15

#### Delayed Write Cycle\*18

t RC

t RAS

t RP

RAS

t CSH

t CRP

t RCD

t T

t RSH

t CAS

CAS

t ASR t RAH

t ASC t CAH

Address

Row

Column

t RCS

t CWL

t RWL

t WP

WE

t DZC

t DS

t DH

Din

High-Z

Din

t DZO

t OEH

t OED

OE

t OEZ

t CLZ

Dout

High-Z

Invalid Dout

Data Sheet E0156H10

16

CAS

Address

WE

Din

OE

#### Read-Modify-Write Cycle\*18

t RWC

t RAS

t RP

t T

t RCD

t CAS

t CRP

t RAD

t ASR tRAH t ASC t CAH

Row

Column

t RCS

t CWD

t AWD

t RWD

tCWL t RWL

t WP

t DZC

t DH

t DS

High-Z

Din

t DZO

t OED

t OEA

t OEH

t CAC

t AA

t RAC

t OEZ

t OHO

Dout

High-Z

t CLZ

RAS

Data Sheet E0156H10

Dout

17

#### RAS-Only Refresh Cycle

t RC

t RAS t RP

t T

t CRP

t RPC

t CRP

t ASR t RAH

Row

t OFR

t OFF

High-Z

RAS

CAS

Address

Dout

Data Sheet E0156H10

18

#### CAS-Before-RAS Refresh Cycle

t RP

t RC

t RAS

t RP

t RPC

t CSR

t T

t CHR

t RPC t CRP

t CP

t WRP t WRH

t CP

t OFR

t OFF

High-Z

RAS

CAS

WE

Address

Dout

Data Sheet E0156H10

19

CAS

Address

WE

Din

OE

Dout

#### Hidden Refresh Cycle

t RC t RC t RC

t RAS

t RP

t RAS t RP t RAS

t RP

t T

t RSH

t CHR

t CRP

t RCD

t RAD

t RAL

t ASR t RAH t ASC t CAH

Row

Column

t WRH

t

RCS

t RRH

t WRP

t

WRP

tWRH

t RRH

t RCH

t DZC

t WED

t CDD

t RDD

High-Z

t DZO

t OED

t OEA

t CAC

t AA

t RAC

t OEZ

t WEZ

t OHO

t CLZ

t OFF

t OH

Dout

t OFR

t OHR

RAS

Data Sheet E0156H10

20

#### EDO Page Mode Read Cycle



tRNCD

t RP

t RASP

t HPC

t

T

t

t HPC

t HPC

t CPRH

tCRP

CSH

tCP

tCP

t CP

t

RSH

CAS t CAS t CAS tCAS tCAS

tRCHR

tRCHC

tRCS

tRCH RCS

t

t

RRH

t

RCH

WE

tASR

tRAH tASC tCAH

tASC t CAH

tASC t CAH

tASC

t RAL

t CAH

t WED

Address

Row

Column 1

t CAL

Column 2

t CAL

Column 3

t CAL

Column 4

t CAL

tDZC

tRDD

tCDD

Din

High-Z

tDZO

tCOL

tCOP

tOED

OE

OEA

tCAC

tAA

tRAC

t

tCPA

tCPA

tAA

CAC

t

OEZ

tCPA

tAA

tCAC

t

t

AA

tWEZ

tOHO

tOEZ

tOEA

tDOH

t

tCAC

tOEA

OHO

tOFR tOHR tOEZ

tOHO tOFF

tOH

Dout

Dout 1

Dout 2

Dout 2

Dout 3

Dout 4

RAS

Data Sheet E0156H10

21

#### EDO Page Mode Early Write Cycle

tRASP

tRP

tT

tCSH

tHPC

tRCD tCAS tCP tCAS tCP

tRSH

tCAS

tCRP

tASR tRAH

tASC tCAH

tASC tCAH

tASC tCAH

Row

Column 1

Column 2

Column N

tWCS tWCH

tWCS tWCH

tWCS tWCH

tDS tDH

tDS tDH

tDS tDH

Din 1

Din 2

Din N

RAS

CAS

Address

WE

Din

Dout

High-Z\*

\* t WCS t WCS (min)

Data Sheet E0156H10

22

#### EDO Page Mode Delayed Write Cycle\*18

t RASP

t RP

t T

t CP

t CSH

t RCD t CAS

t CP

t CRP

t HPC

t CAS

t RSH

t CAS

t RAD

t ASR

t RAH

t ASC

t CAH

t ASC

t CAH

t ASC

t CAH

Address

Row

Column 1

Column 2

Column N

t CWL t CWL t CWL

t RWL

t RCS

t RCS

t RCS

WE

t WP

t DZC t DS

t WP

t DZC t DS

t WP

t DZC t DS

t DH t DH t DH

Din

Din 1

t DZO

Din 2

t DZO

Din N

t DZO

t OED

t OEH

t OED

t OEH

t OED

t OEH

OE

t CLZ

t CLZ

t CLZ

t OEZ t OEZ t OEZ

Dout

High-Z

RAS

CAS

Invalid Dout

Invalid Dout

Invalid Dout

Data Sheet E0156H10

23

#### EDO Page Mode Read-Modify-Write Cycle\*18

t RASP

t RP

t T

t HPRWC

t CP t CP

t RCD t CAS

t RSH

t CAS

t CRP

t CAS

t RAD

t ASR t ASC

t RAH t CAH

t ASC

t CAH

t ASC

t CAH

Address

Row

Column 1

Column 2

Column N

t RWD t CWL

t AWD

t CWD

t CPW

t AWD

t CWD

t CWL

t CPW t CWL

t RCS

t RCS

t AWD

t CWD

t RWL

WE

t RCS t WP

t DZC t DS

t WP

t DZC t DS

t WP

t DZC t DS

t DH t DH t DH

Din

Din 1

t DZO

t OEH

Din 2

t DZO

t OEH

Din N

t DZO

t OED

t OED

t OED

t OEH

OE

t OHO

t OHO

t OHO

t OEA

t CAC

t AA

t RAC

t CLZ

t OEA

t CAC

t OEA

t CAC

t AA

t CPA

t AA

t CPA

t OEZ

t CLZ

t OEZ

t CLZ

t OEZ

High-Z

Dout

RAS

CAS

Dout 1

Dout 2

Dout N

Data Sheet E0156H10

24



t RP

t RASP

tT

tCRP

tCP

tCP

t CP

t CAS

t CSH

t CAS

tCAS

tCAS

tRCD

tWCS

tRSH

tWCH

tRCS

tRCS

tRRH tRCH

tCPW tAWD

tWP

tASR tRAH

tASC tCAH

t

ASC

t CAH

tASC t CAH

tASC

t RAL

t CAH

Row

Column 1

Column 2

Column 3

Column 4

t CAL t CAL t CAL

t CAL

t

DS

tDH

tDS

tDH

tRDD tCDD

Din 1

High-Z

Din 3

tOED

tWED

AA

tOEA

tCPA

t

tCPA tOFR

tCPA

tAA

tOEZ

t

tWEZ

AA

tCAC

t

OEZ

tOHO

tCAC

tCAC tOHO

tDOH

tOEA

tOFF

tOH

Dout

Dout 2

Dout3

Dout 4

RAS

CAS

WE

Address

Din

OE

Data Sheet E0156H10

25



tRNCD

t RP

t RASP

tT

t CSH

tCP

t CP

tCRP

tRCD

t CAS

tRCHR

t CAS

tCAS

tCAS

tRSH

tRCS

tRCS

RCH

t tWCS tWCH

t RCS

tRRH tRCH

WE tCPW tWP

t RAL

tASR

tASC tRAH

tCAH

t

ASC t CAH

tASC t CAH

tASC

t CAH

Address

Row

Column 1

t CAL

Column 2

t CAL

Column 3

t CAL

Column 4

t CAL

tDS

tDS

tDH

tDH

tRDD tCDD

Din

High-Z

Din 2

Din 3

tOED

tOED

tCOP

t

WED

tCOL

OE

tAA tOEA

tCAC

tRAC

tOEZ

tOEA

tCPA

tAA

tCAC

tOHO

tOEZ

tOHO

tCPA

tAA

tCAC

OEA

tOFR

tWEZ

tOEZ OHO

tOFF

tOH

Dout 4

t

t

Dout

Dout 1

Dout3

RAS

CAS

Data Sheet E0156H10

26

t RP t RASS t RPS

t RPC

t CP

t T

t CRP

t CSR

t CHS

t WRP t WRH

t OFR

t OFF

High-Z

RAS

CAS

WE

Dout

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27



9.40  0.25

3.50  0.26

0.80 +0.25

–0.17

2.85  0.12

### Package Dimensions

**HM5117805J/LJ Series** (CP-28DA)



18.54 Max

28

15

1.27

0.10

Unit: mm

18.17

1

0.74

14

1.30 Max

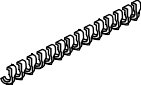
0.43  0.10

0.41  0.08

Dimension including the plating thickness Base material dimension

10.16  0.13

11.18  0.13



|  |  |
| --- | --- |
| Hitachi Code | CP-28DA |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Weight (reference value) | 1.16 g |

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28



6.79  0.18

3.50  0.26

0.90  0.26

2.45 + 0.25

– 0.36

**HM5117805S/LS Series** (CP-28DNA)



18.84 Max

28

15

0.10

Unit: mm

18.41

1

0.74

14

1.165 Max

0.43  0.10

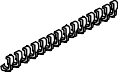
0.41  0.08

Dimension including the plating thickness Base material dimension

1.27

7.62  0.12

8.51  0.12



|  |  |
| --- | --- |
| Hitachi Code | CP-28DNA |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.95 g |

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29

0.10

0.80



0.50  0.10

1.20 Max

10.16

0.145  0.05

0.125  0.04

0.13  0.05

0.68

**HM5117805TT/LTT Series** (TTP-28DA)



Unit: mm

18.41

18.81 Max

28

15

1

1.27

14

0.42  0.08

0.40  0.06

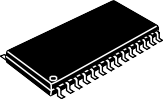
0.21 M

1.15 Max

11.76  0.20

0 – 5

Dimension including the plating thickness Base material dimension



|  |  |
| --- | --- |
| Hitachi Code | TTP-28DA |
| JEDEC | Conforms |
| EIAJ | — |
| Weight (reference value) | 0.43 g |

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30

0.10



0.50  0.10

1.20 Max

7.62

0.145  0.05

0.125  0.04

0.13  0.05

0.63

**HM5117805TS/LTS Series** (TTP-28DB)



Unit: mm

18.41

18.81 Max

28 15

1

1.27

14

0.42  0.08

0.40  0.06

0.21 M

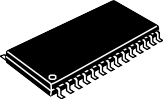
0.80

1.15 Max

9.22  0.2

0 – 5

Dimension including the plating thickness Base material dimension



|  |  |
| --- | --- |
| Hitachi Code | TTP-28DB |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.35 g |

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